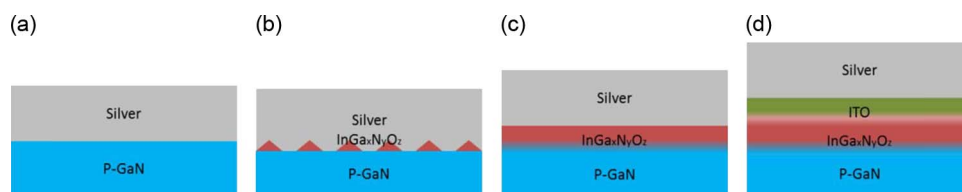


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Modulating Ohmic Contact Through $\text{InGa}_x\text{N}_y\text{O}_z$ Interfacial Layer for High-Performance InGaN/GaN-Based Light-Emitting Diodes

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Abstract: We report the improved performance of InGaN/GaN-based light-emitting diodes (LEDs) through the design and the formation of the $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer, which maintains high reflectivity of silver and forms good ohmic contact between pristine silver and p-GaN. The interfacial layer was designed and formed by depositing a thin layer of indium tin oxide (ITO) on top of p-GaN, followed by thermal annealing, to enable the interdiffusion and the intermixing of In, Sn, Ga, O, and N atoms. Both electrical and optical performances of the LED with the optimized $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer are improved, thus achieving the highest wall-plug efficiency, compared with those LEDs with and without ITO layers at operation current.

Index Terms: Indium tin oxide (ITO), $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer, light-emitting diode (LED), ohmic contact.

1. Introduction

The performance of InGaN/GaN-based flip-chip light-emitting diodes (LEDs) has been significantly improved with the increase of light extraction efficiency by designing the reflective contact mirror [1]–[3]. For the flip-chip LEDs, the emitted photons are reflected by the mirror on the p-GaN and extracted out from the backside of LEDs, in which the reflective ohmic contact is critically important. Typically, silver is used as the reflective contact mirror due to its high reflectivity among various metallic reflectors in the visible wavelength range [4]. However, silver has poor adhesion and is difficult to form ohmic contact directly with the p-GaN due to the work function mismatch [5], [6]. Insertion of a Ni layer between silver and GaN can mitigate the adhesion problem, and subsequent annealing in oxygen atmosphere can help to form better ohmic contact [7]. Nevertheless, annealing often causes silver to oxidize and agglomerate, which, in turn, severely

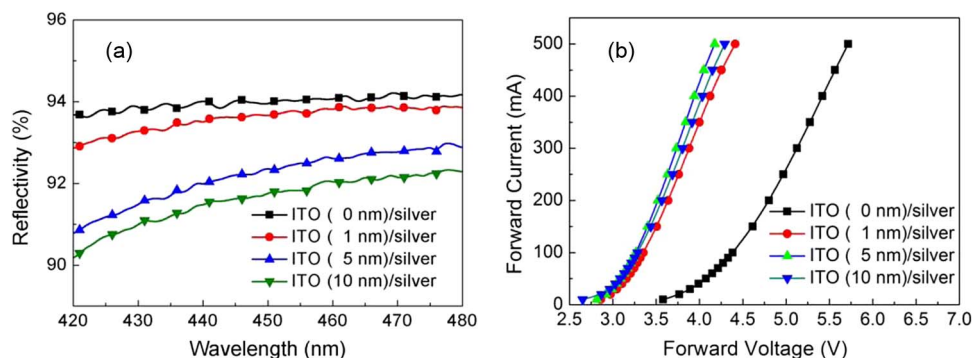


Fig. 1. (a) Reflectivity of mirrors. (b) I – V curve of flip-chip LEDs, with different thin ITO layers.

degrades the mirror performance [8]. On the other hand, the indium tin oxide (ITO) insertion layer between p-GaN and the silver mirror is often used as ohmic contact for its superior performance, such as high electrical conductivity, high transparency to visible light, and stable chemical properties [9]–[11]. However, the role of the ITO layer in those LEDs has not been thoroughly investigated, and the underlying physics for ohmic contact formation has not been discussed.

In this work, we design a set of experiment with the incorporation of a thin ITO layer on the p-GaN surface and investigate the interfacial layer that forms between the p-GaN and pure silver. With the optimized parameters in this study, we have achieved high performance mirror with high reflectivity which is almost the same as the pristine silver layer, and low contact resistance which is comparable to Ni/Ag or thick ITO/Ag combinations. The formation of $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer is studied using various characterization methods, and a model is proposed to illustrate the mechanism for ohmic behavior.

2. Experimental Details

The epitaxial layers of LEDs were grown by metal-organic chemical-vapor deposition (MOCVD) system on patterned sapphire substrates. The dominant wavelength emitted by the LEDs was 450 nm. The details of the growth conditions and the layer structures can be found in our previous work [12]. After MOCVD growth, the LEDs were fabricated into chips by a series of standard fabrication techniques. First, one wafer was cut into four pieces, while three pieces of wafers were deposited with ITO of 1 nm, 5 nm, and 10 nm, respectively by e-beam evaporator, and the last one was left as the reference. Then, the samples underwent annealing at 630 °C in oxygen ambient for 1 minute. After that, a layer of Ag (200 nm)/Ti (50 nm) was deposited by sputtering on top as the reflective mirror of the contact. The mesa size was defined as $1 \times 1 \text{ mm}^2$ and etched by inductively coupled plasma (ICP). The electrodes for the devices which were composed of Ti/Ag/Ti/Au were deposited by e-beam evaporator. The samples for reflectivity measurement were prepared by depositing thin ITO layers/Ag mirror on top of double-side polished sapphire substrates, and the measurements were conducted using a Perkin Elmer Lambda 950 UV/VIS/NIR Spectrophotometer system. The current-voltage (I – V) characteristic was measured by a SC-200-mm probe station and the optical output power was measured using an ocean optics spectrometer, which was attached with an integrating sphere. Surface morphologies of ITO layers with different thicknesses were characterized using atomic force microscopy (AFM) (scanning Probe Microscope Model DI dimension V), surface sheet resistance was measured through four-probe method by a sheet resistance n resistivity equipment, and the binding energies of elements in the surface material were achieved by a home-made X-ray photoelectron spectroscopy and Ultraviolet photoelectron spectroscopy (XPS and UPS) system.

3. Results

Fig. 1(a) shows the reflectivity of thin ITO layers with various thicknesses after silver deposition. The reflectivity of the mirror with 1 nm ITO insertion layer is almost the same as that of the

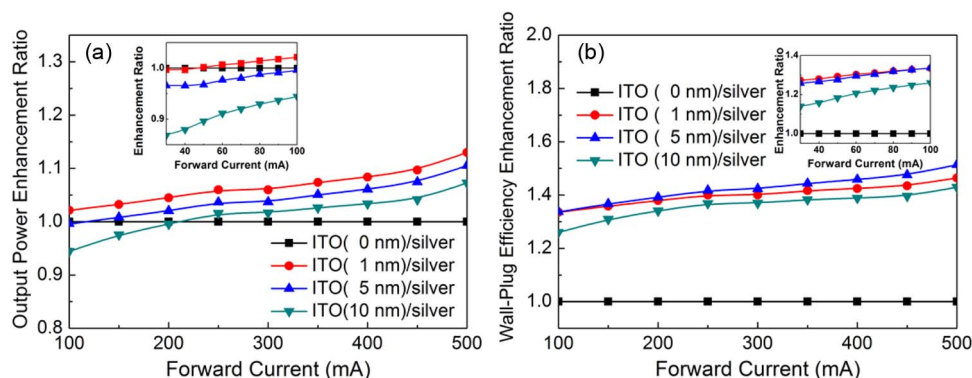


Fig. 2. (a) Optical output power and (b) wall-plug efficiency enhancement ratio for samples with different ITO layers when compared with the reference. (Inset) Same curve at low current range from 30 to 100 mA.

pristine silver mirror. As the thickness of ITO insertion layer increases to 5 nm and 10 nm, the reflectivity of the mirror starts to decrease. Even though the change of the reflectivity value is small here due to the thin thickness of ITO insertion layers, it clearly shows the trend that with thicker ITO insertion layer, the reflectivity of the mirror degrades. Therefore, the ITO insertion layer should be made as thin as possible for better optical performance. The optical performance of the mirrors with thin ITO insertion layers here is much better than that of annealed Ni/Ag mirror, for which the reflectivity is even lower than 80% at 450 nm [13]. The I - V characteristic of flip-chip LEDs with different thicknesses of ITO insertion layers is shown in Fig. 1(b). From the I - V curve, we can see that without ITO insertion layer, the forward voltage is much higher, indicating the poor ohmic contact formation between silver mirror and p-GaN. When the thin ITO layer is inserted, the I - V performance is greatly improved even when the thickness is just 1 nm. The lowest forward voltage among the three samples with ITO layers happens when the thickness of ITO insertion layer is 5 nm. The mechanism about why the ITO with 5 nm can achieve the best electrical performance will be discussed in the following part.

Fig. 2(a) shows the optical output power enhancement ratio of LEDs with various thin ITO insertion layers when compared with the reference from 100 mA to 500 mA, while the inset shows the value with current from 30 mA to 100 mA. For the lower current range in the inset, the optical power for LED with 10 nm ITO is lower than other samples for its lowest mirror reflectivity. With increasing current, the LED without ITO layer gradually becomes smaller than others, since the sample has largest forward voltage and thus more heat will be generated in the process [14]. Among the three samples with different ITO insertion layers, the one with 1 nm ITO has the largest optical output power, which is consistent with the reflectivity of the ITO mirrors shown in Fig. 1(a). Fig. 2(b) shows the wall-plug efficiency enhancement ratio for samples with different ITO layers when compared with the reference, with inset showing the curve at low current from 30 mA to 100 mA. All the samples with ITO layers present obviously superior performance than the one without ITO layer in the whole injection current range. At operation current, for all the samples with ITO layers, the one with 5 nm shows better performance than other results due to reduced forward voltage. Apparently the insertion of thin ITO layers between silver and p-GaN surface changes the electrical property while maintains the high optical performance of the silver mirror and thus leads to the improved overall device performance. The optimized thickness of ITO is 5 nm instead of 1 nm or 10 nm. Thus, the mechanism behind the phenomenon is worth to be investigated.

Fig. 3 shows the atomic force microscopy (AFM) images of the thin ITO layers deposited on p-GaN surface before and after annealing. For the 1 nm ITO layer before annealing as shown in Fig. 3(a), the surface is featured by step-flow structures [15], which originates from the p-GaN surface, indicating the conformal deposition of the thin ITO layer. When the ITO layer increases to 5 nm and 10 nm, the surface morphology turns into grain structures, as shown in

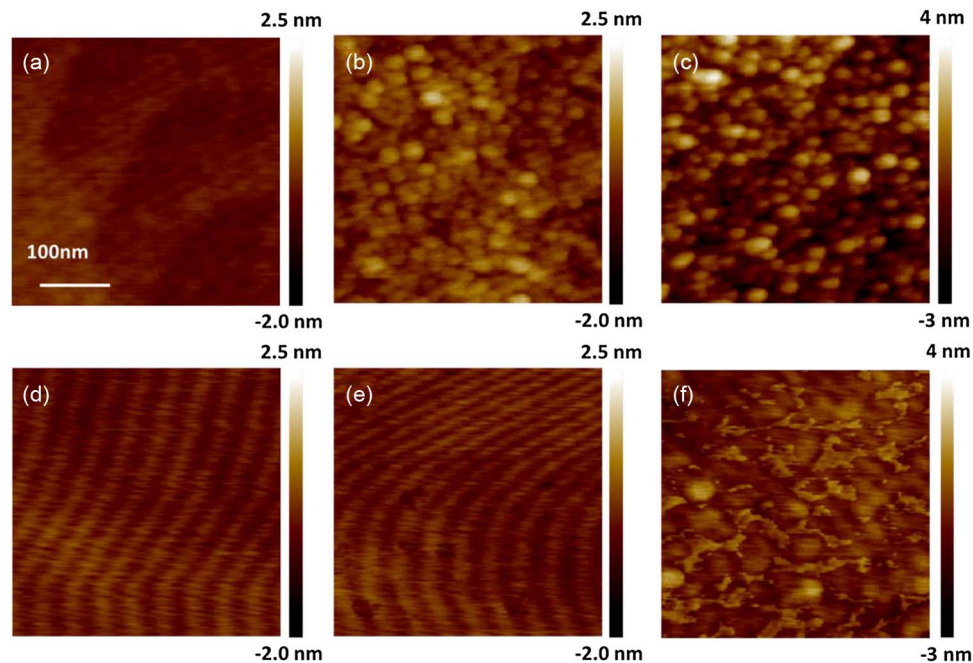


Fig. 3. AFM images of p-GaN surface after ITO deposition with 1 nm ITO (a) before and (d) after annealing, 5 nm ITO (b) before and (e) after annealing, and 10 nm ITO (c) before and (f) after annealing.

TABLE 1

Sheet resistance of thin ITO layers on top of p-GaN before and after annealing (Ω/\square)

Type	Non-annealed	Annealed
ITO (1 nm)	2.858 M	115.9 K
ITO (5 nm)	153.5 K	22.88 K
ITO (10 nm)	168.2 K	1.556 K

Fig. 3(b) and (c), which shows that as the ITO thickness increases, the conformality is lost, and the granular nature of ITO layers is dominated. It is interesting to note that after annealing the surface morphology of the sample with 1 nm ITO layer maintains the step-flow characteristic as shown in Fig. 3(d), while the surface morphology of the sample with 5 nm ITO layer turns from granular structures into step-flow structures as shown in Fig. 3(e). Even for the sample with 10 nm ITO layer, the surface morphology also seems to experience changes from granular characteristic to step-flow nature as shown in Fig. 3(f). This change in the surface morphology after annealing allows us to reasonably assume that during annealing, 1) the process of interfacial atomic inter-diffusion and inter-mixing takes place; 2) for 1 nm and 5 nm ITO layers, the atomic inter-diffusion and inter-mixing is thorough meaning that the whole ITO layer has turned into the interfacial layer and no pure ITO layer, is left; and 3) for the 10 nm ITO layer, only underlying part of the layer turns into the interfacial layer, and the rest of the top ITO layer is left intact. The conjecture of the formation of the interfacial layer by the atomic inter-diffusion and inter-mixing has been supported by other experimental results as follows.

The sheet resistance of the thin ITO layers deposited on p-GaN surface before and after annealing is listed in Table 1. Before annealing, the sheet resistance for the sample with 1 nm ITO layer is around 2.9 M Ω/\square , while it is around 150 K Ω/\square , for the samples with 5 and 10 nm ITO layers. The sheet resistance of 2.9 M Ω/\square is at the same order of magnitude with the value of p-GaN, which implies that the probe may penetrate the 1 nm ITO layer during the measurement.

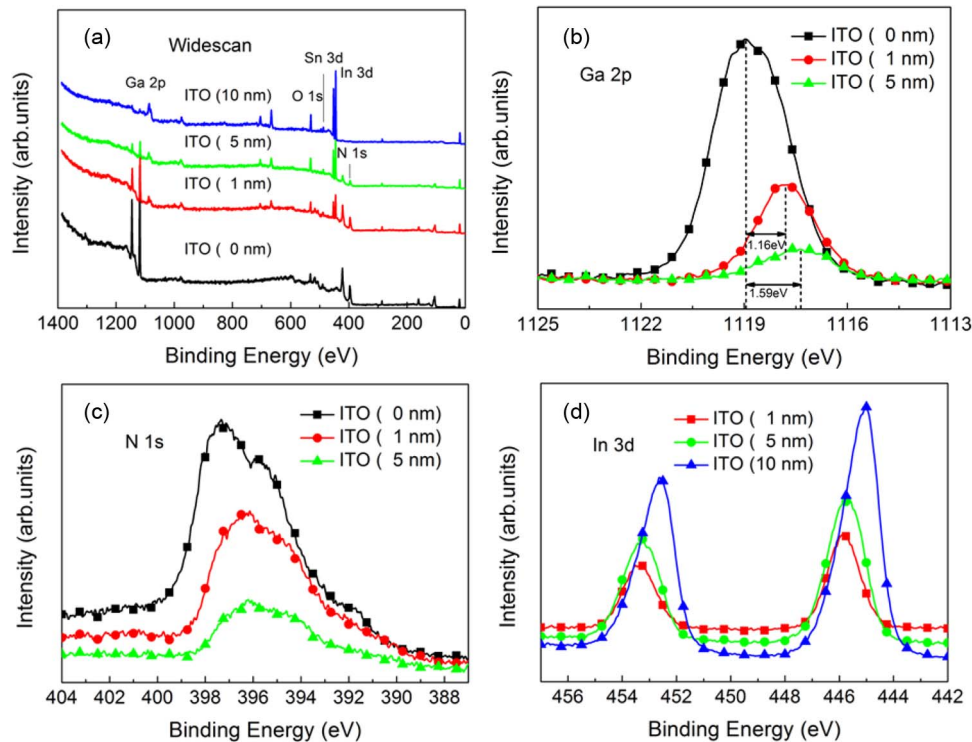


Fig. 4. (a) XPS wide-scan spectrum of all the elements. (b) Ga 2p core spectra. (c) N 1s core spectra. (d) In 3d core spectra.

The sheet resistance of $150 \text{ K } \Omega/\square$ is the typical value for the un-annealed ITO thin layers. After annealing, the sheet resistances for all the three samples become much smaller. For the sample with 1 nm ITO layer the sheet resistance is around $116 \text{ K } \Omega/\square$, more than one order of magnitude lower than that before annealing. This strongly indicates that a highly conductive interfacial layer is formed on the p-GaN surface during the annealing through atomic inter-diffusion and inter-mixing. The sheet resistance becomes even smaller as the ITO layer thickness increases, which may imply that the interfacial layer becomes more conductive due to the larger amount of ITO supply during the interfacial layer formation. We have to bear in mind that for the sample with 10 nm ITO, a certain thickness of ITO has been left, as shown in Fig. 3(f), which also contributes to the conductivity and, thus, results in the lowest sheet resistance together with the interfacial layer.

In order to analyze the chemical properties of the interfacial layer, XPS examination was performed on the samples after annealing. Wide-scan spectrum of the binding energies for all the samples is shown in Fig. 4(a). For the sample without ITO coating, only Ga 2p and N 1s signals can be observed which originate from the clean GaN surface. For samples coated with 1 nm and 5 nm ITO thin layers, the signals from Ga 2p and N 1s can still be observed even though they become weaker as the ITO thickness increases. In addition, signals from O 1s, Sn 3d and In 3d have also been observed. For the sample coated with 10 nm ITO layer, signals from O 1s, Sn 3d and In 3d are clearly observed while the signal from Ga 2p is very weak and the signal from N 1s is hardly observed. From these observations, it can be deduced that when the ITO thickness is more than 10 nm, the surface part is pure ITO layer and only bottom part of the ITO layer participates in the atomic inter-diffusion and inter-mixing process with the underlying GaN layer and converts into the interfacial layer. When the ITO thickness is as thin as 1 nm and up to 5 nm, the atomic inter-diffusion and inter-mixing consumes the whole ITO layer and the surface region of the underlying p-GaN transforms them into the interfacial layer. The details in the binding energy change for Ga 2p, N 1s and In 3d of the samples are shown in Fig. 4(b)–(d),

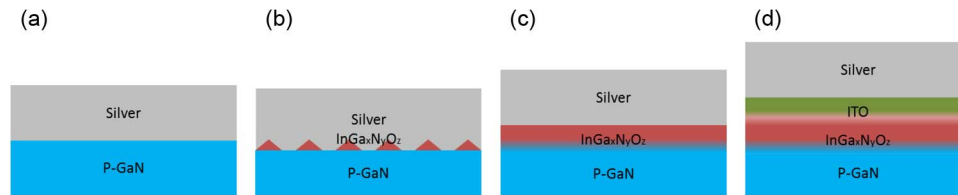


Fig. 5. Schematic of the element mixing for contact mirror with (a) no ITO layer; (b) 1-nm annealed ITO layer, with a formation of island-like $\text{InGa}_x\text{N}_y\text{O}_z$ layer; (c) 5-nm annealed ITO layer, with a formation of $\text{InGa}_x\text{N}_y\text{O}_z$ layer; and (d) 10-nm annealed ITO layer.

respectively. It can be seen from Fig. 4(b) and (c) that the binding energies for Ga 2p and N 1s for the samples coated with 1 nm and 5 nm ITO layers shift to lower energy, compared to the sample without ITO coating. On the other hand, the binding energies for In 3d for the samples coated with 1 nm and 5 nm ITO layers are quite close to each other but much larger than that for the sample coated with 10 nm ITO layer, as shown in Fig. 4(d). The changes in the binding energy of Ga 2p, N 1s and In 3d for samples coated with 1 nm and 5 nm ITO layers with respect to the samples without ITO coating and coated with 10 nm ITO layer clearly show that the interfacial layer composes of Ga, In, N, and other elements with inter-atomic chemical bonds different from those in the original ITO and GaN layers. The changes in the binding energy are in favor of the formation of ohmic contact. For example, the shift of the binding energy of Ga 2p in the interfacial layer to lower energy with increasing thickness reflects that the surface Fermi level shifts to the valence band edge and results in a reduction in the band bending of p-GaN [16], [17].

Based on the discussion above, we propose the following model to explain the ohmic contact formation of the silver contact mirror inserted with thin ITO layers. As illustrated in Fig. 5, schematic diagrams of all the elements for the contact mirrors are drawn to show the element profile distribution. In Fig. 5(a), since no annealing is applied after silver deposition, no inter-diffusion happens and the interface is sharp and smooth. For Fig. 5(b) and (c), the atomic inter-diffusion and inter-mixing between the p-GaN and ITO is very thorough, which means the thin ITO layers are totally mixed with p-GaN. In the process, Ga will diffuse out to form a thin interfacial layer composed of $\text{InGa}_x\text{N}_y\text{O}_z$ and leave Ga + vacancies at the surface of p-GaN [18]. However, small islands made of $\text{InGa}_x\text{N}_y\text{O}_z$ are formed instead of continuous film when the thickness of ITO is as thin as 1 nm, as shown in Fig. 5 (b). Some of the p-GaN is still in direct contact with silver, which contributes to extra forward voltage when compared with the sample with 5 nm ITO. This can also demonstrate the high sheet resistance of sample with 1 nm ITO when compared with that of 5 nm ITO. In Fig. 5(d), bottom part of ITO will mix with p-GaN and top part will be left intact. The different profiles of the p-GaN surfaces with ITO layer of different thickness will result in different electrical properties as shown in the following analysis.

Fig. 6(a) and (b) shows the energy band diagrams of samples with and without the interfacial layer at equilibrium state. An ohmic contact between a metal and p-GaN can only be formed when the work function of metal is larger than the p-type semiconductor [19]. Since the work function of silver and p-GaN are 4.25 eV [20] and 7.5 eV [21], respectively, a Schottky contact is formed between the silver and p-GaN, as shown in Fig. 6(a). The Schottky barrier height (SBH) for the contact is 3.25 eV. Therefore, carriers are very difficult to flow through the contact. For the LED with a thin ITO layer and subsequently annealed to form the $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer, Ga + vacancies will be generated [18] at the p-GaN surface as stated previously, which results in a decrease of binding energy of Ga 2p core level, as shown in Fig. 4(b). When compared with the sample without ITO, it is noted that the Ga 2p core level shifts towards lower binding-energy side by 1.16 eV for the sample with 1 nm ITO, and 1.59 eV for the sample with 5 nm ITO. The difference of Ga 2p core level binding energy results in a Fermi level down-shift by a value larger than 3.25 eV, which is attributed to the interfacial layer [22]. Since the Fermi level of bulk p-GaN does not change and the interfacial layer is in contact with the p-GaN, the surface energy band shifts upward by more than 3.25 eV. When compared with the reference after contacting with silver, the direction of the band bending at the interface

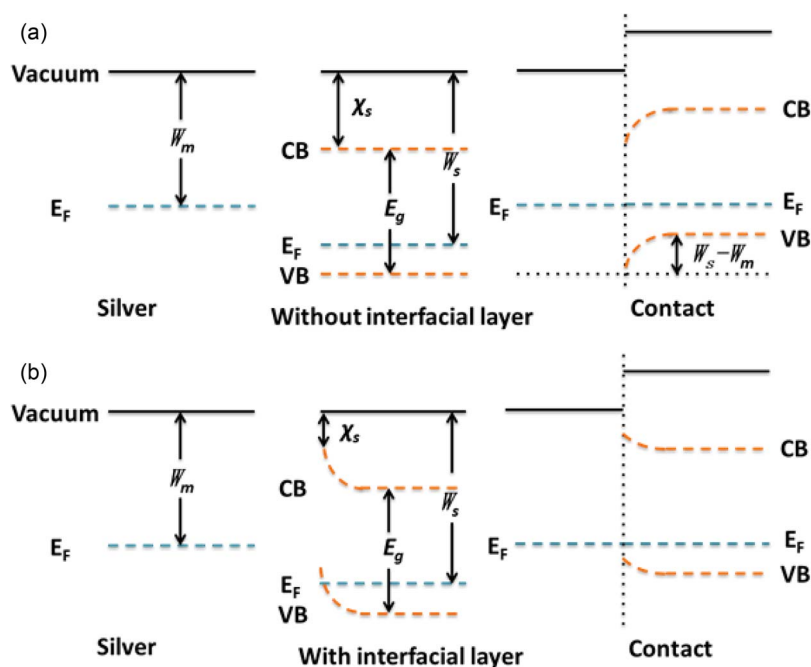


Fig. 6. Schematic of the silver and p-GaN contact with (a) no interfacial layer and (b) $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer.

changes from downward to upward, which facilitates the ohmic contact formation between the p-type semiconductor and metal, as shown in Fig. 6(b). For the sample with 10 nm ITO layer, there still exists an unconsumed ITO layer between silver and the interfacial layer, which will add more parasitic resistance and lead to higher forward voltage, as shown in Fig. 1(b), due to small work function mismatch.

4. Conclusion

In summary, we have designed a set of experiment with the incorporation of a thin ITO layer to facilitate the formation of $\text{InGa}_x\text{N}_y\text{O}_z$ interfacial layer through thermal annealing process. The optimized design allows the formation of a full $\text{InGa}_x\text{N}_y\text{O}_z$ layer that interfaces directly with the p-GaN and pure silver, and in turn preserves the high-reflectivity of the pure silver and high-performance ohmic contact. A InGaN/GaN -based LED that employs this optimized design performs better in both electrical and optical aspects and yields the highest wall-plug efficiency at operation current in this study.

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